Fig.1A

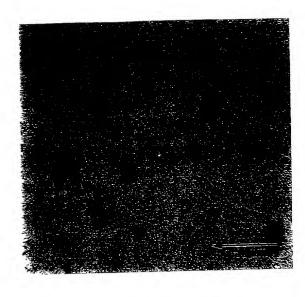


Fig.1B

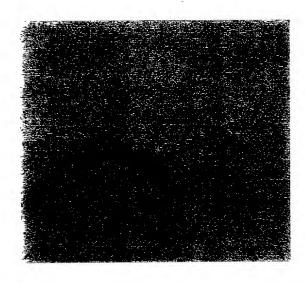


Fig.1C

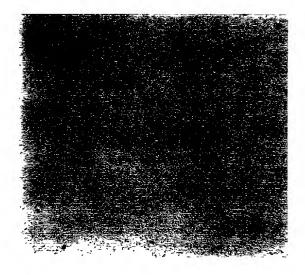


Fig.2A

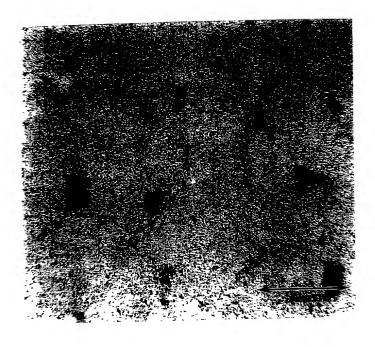


Fig.2B

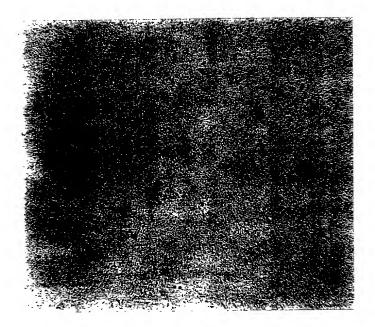


Fig.3A

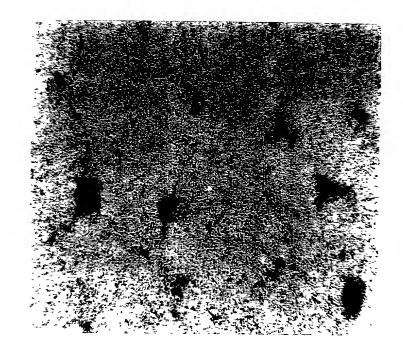
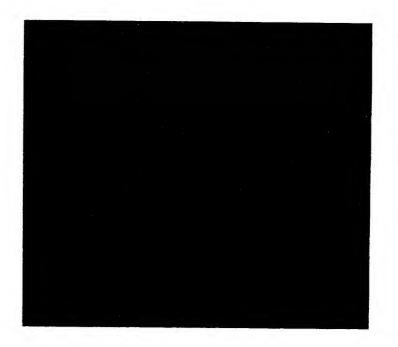


Fig.3B



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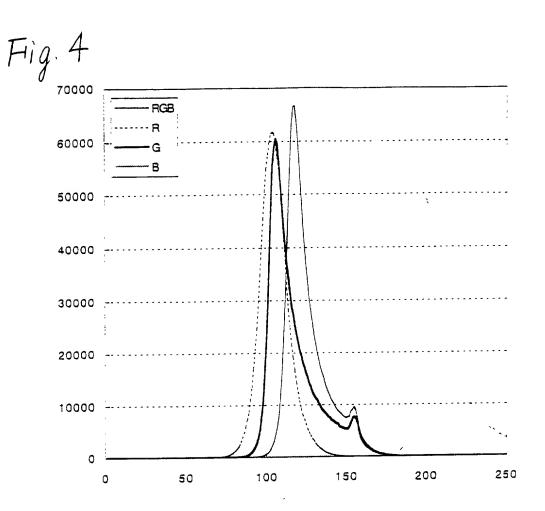


Fig.5A

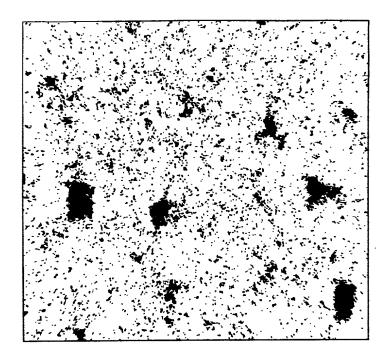
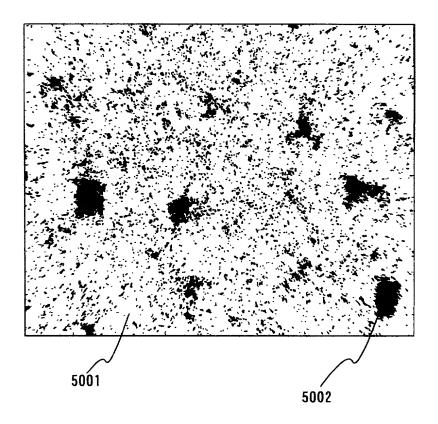
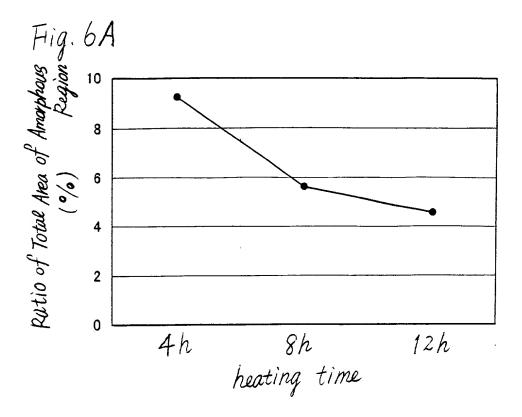
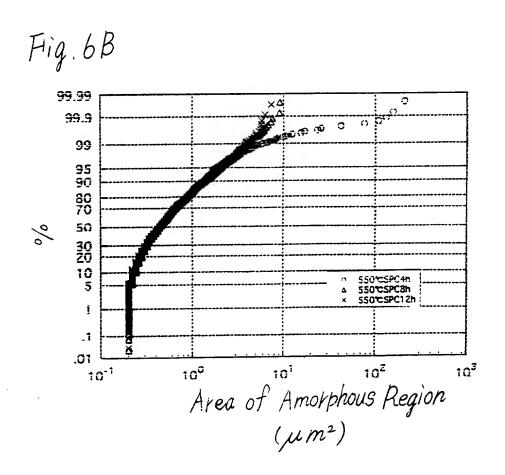
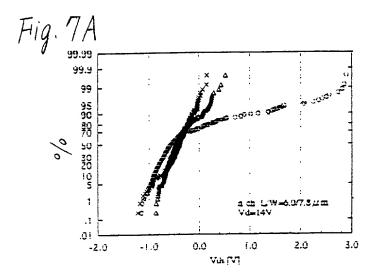


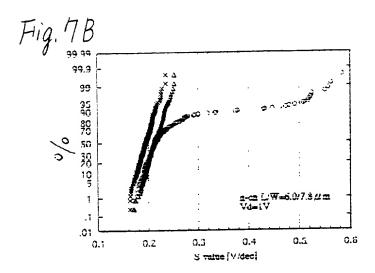
Fig.5B

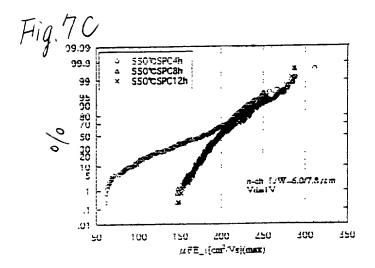


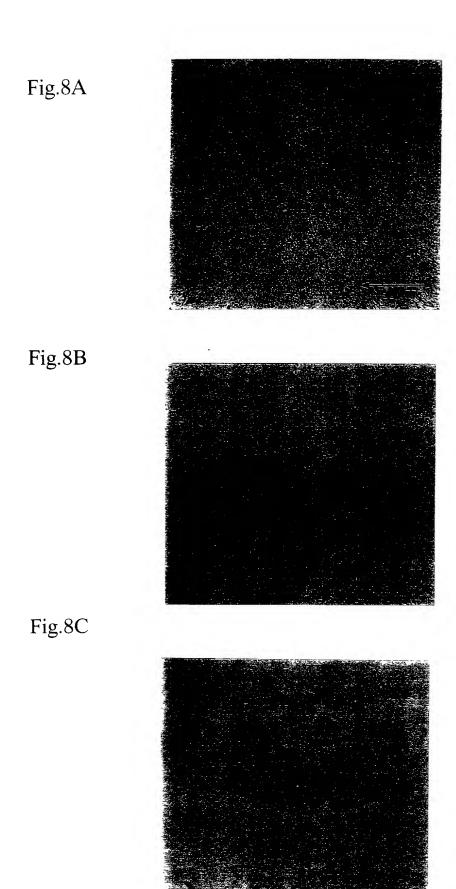


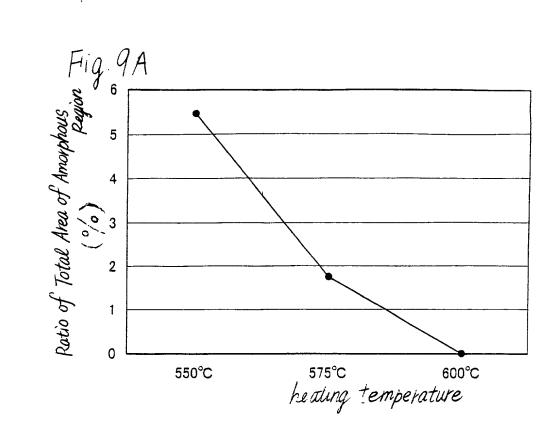


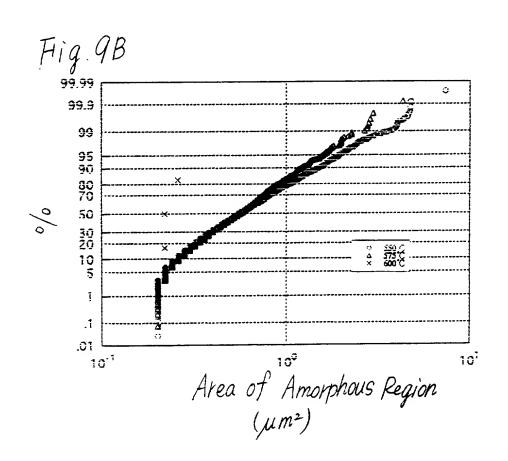


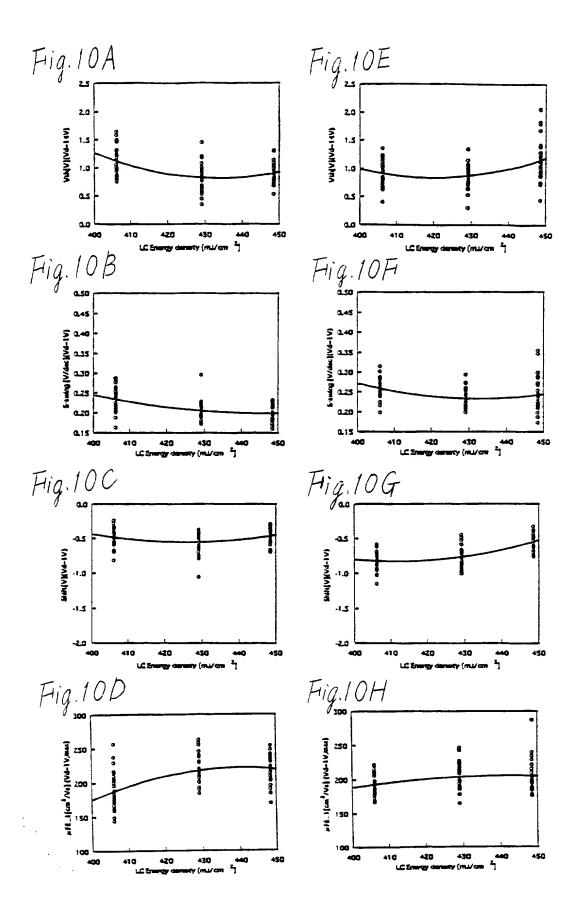


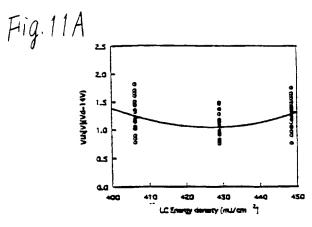


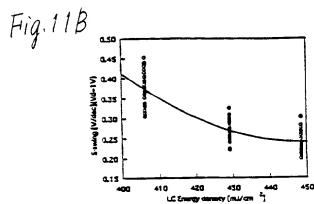


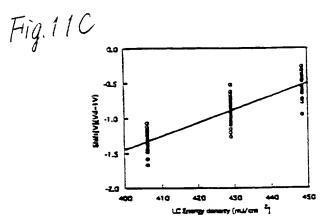


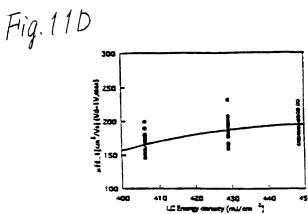












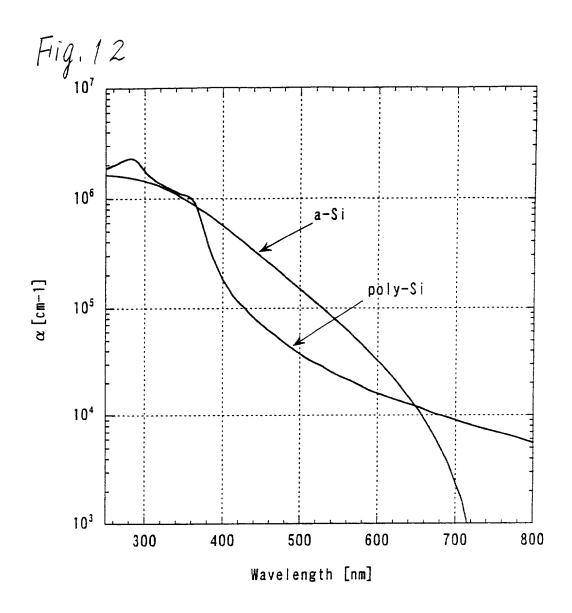
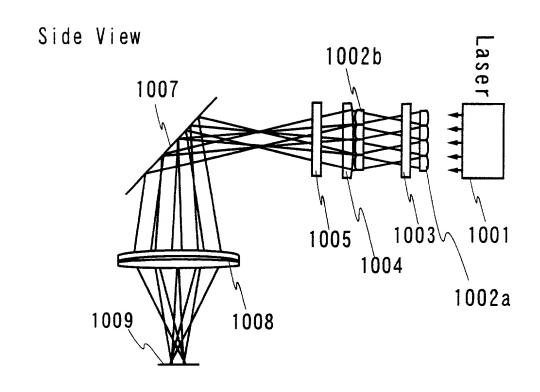
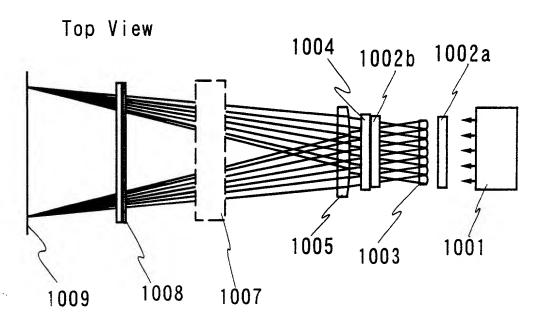


Fig.13





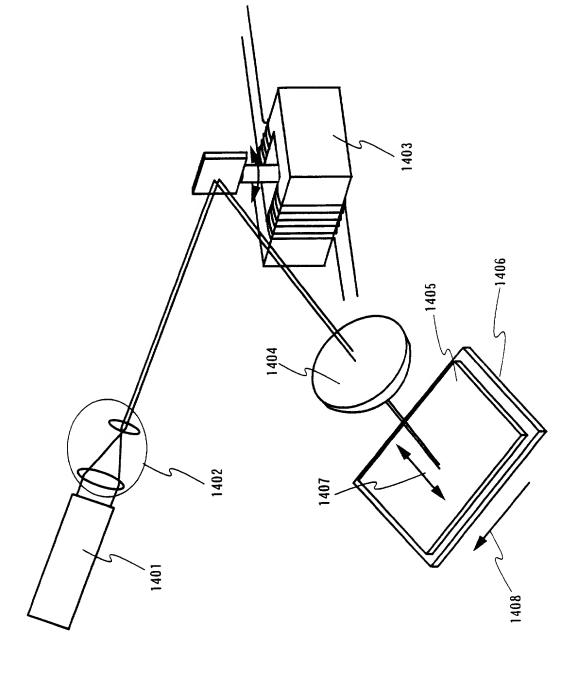
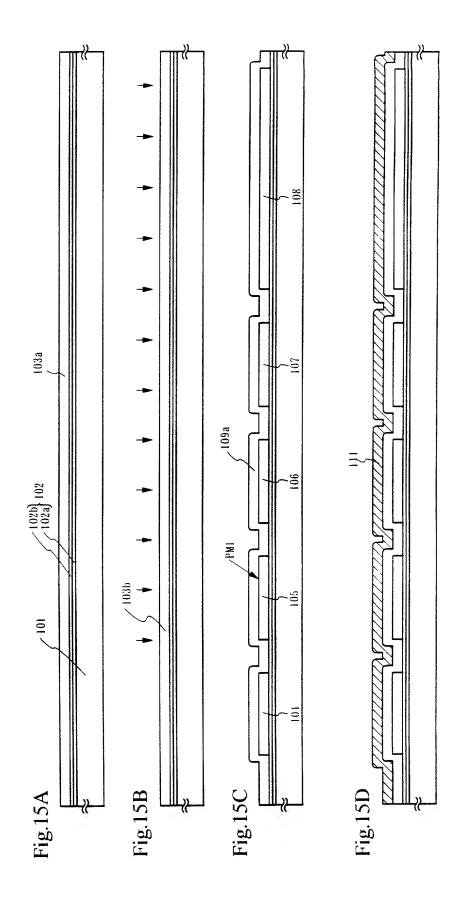
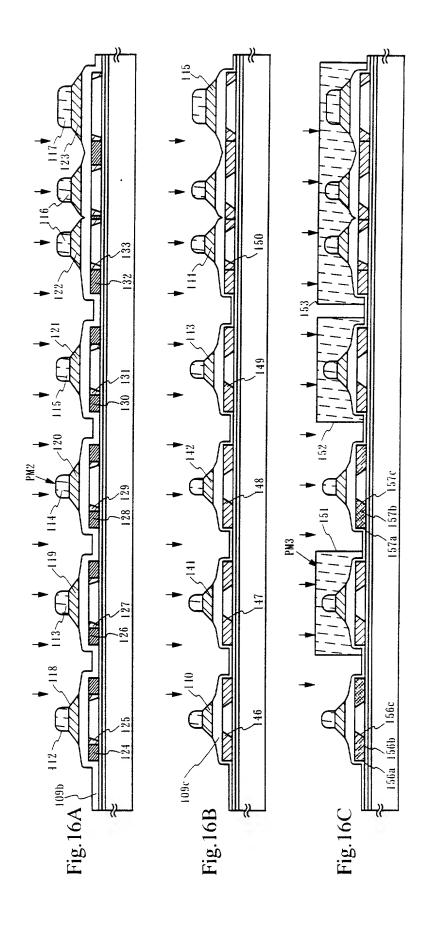
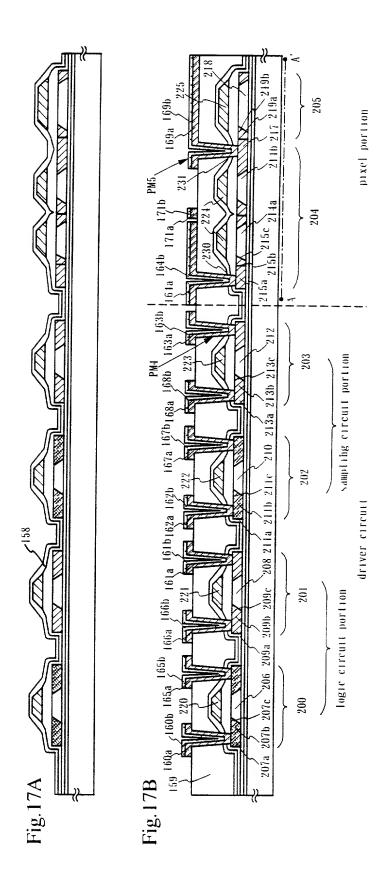
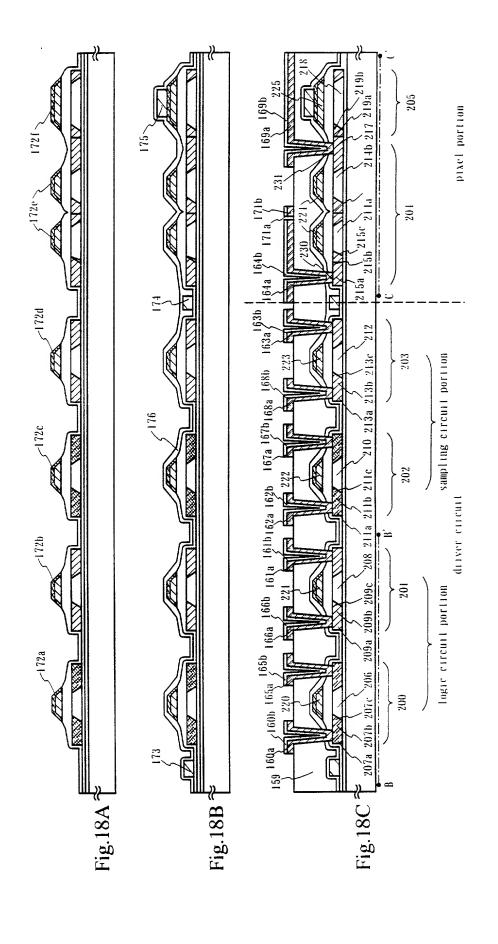


Fig.14









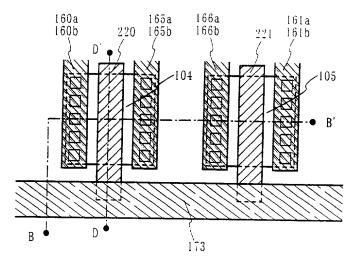


Fig.19A

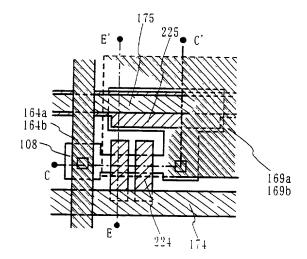
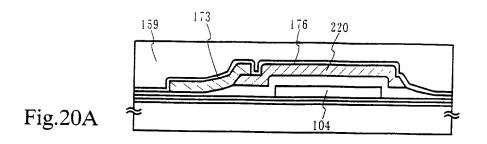
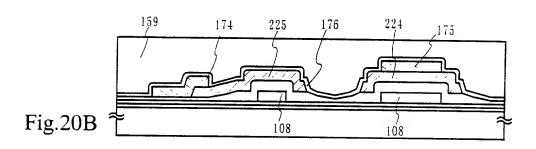
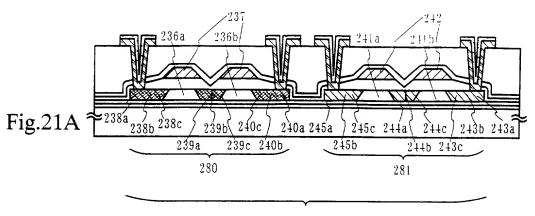


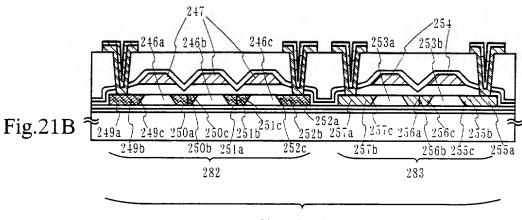
Fig.19B







logic circuit portion



sampling circuit portion

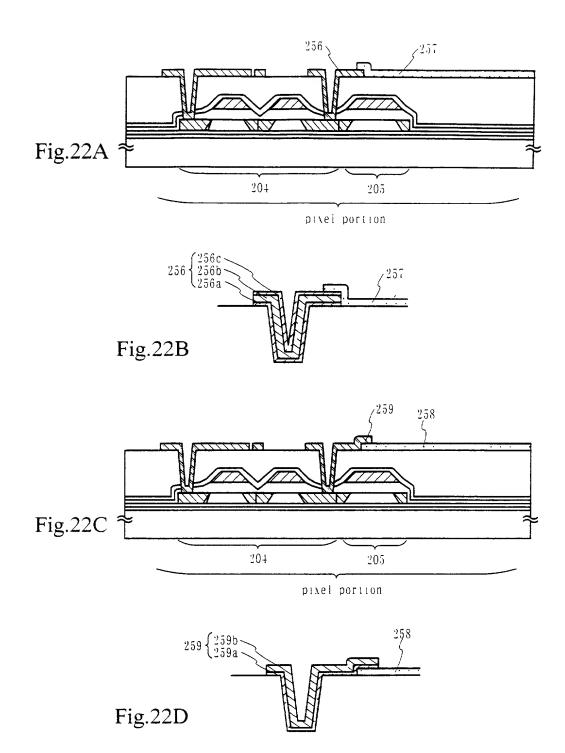
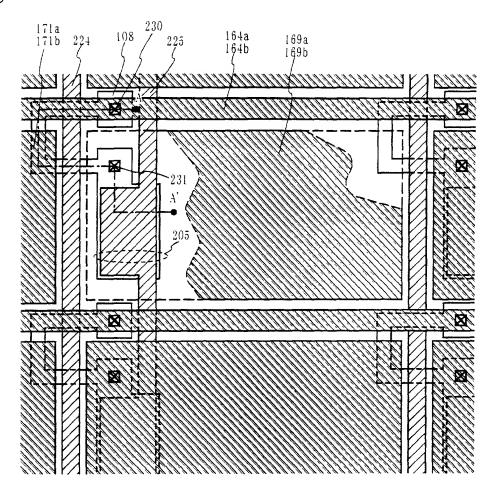
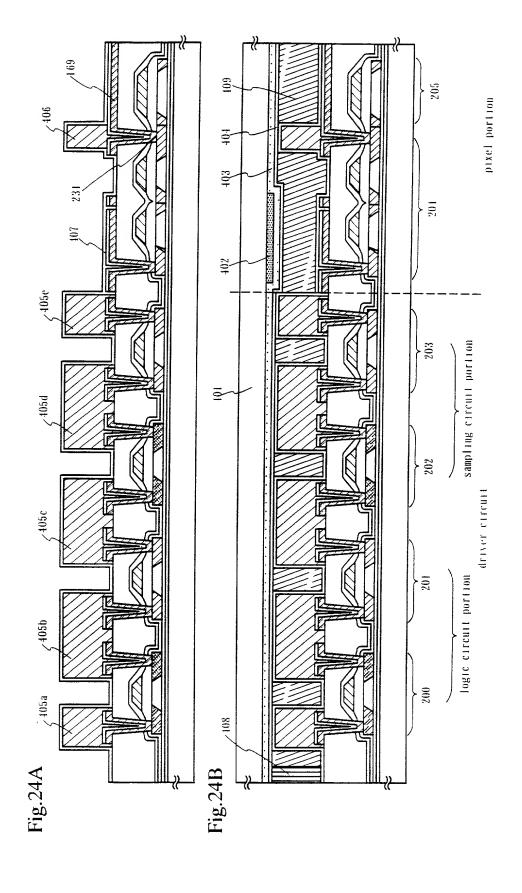


Fig.23





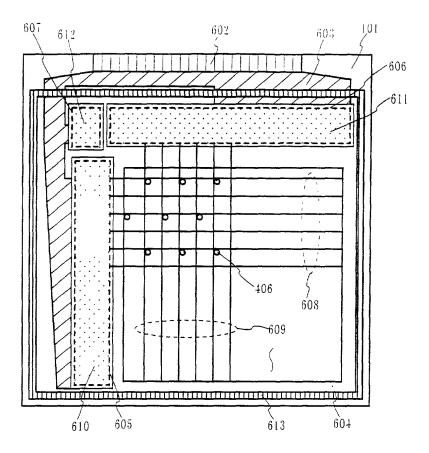


Fig.25

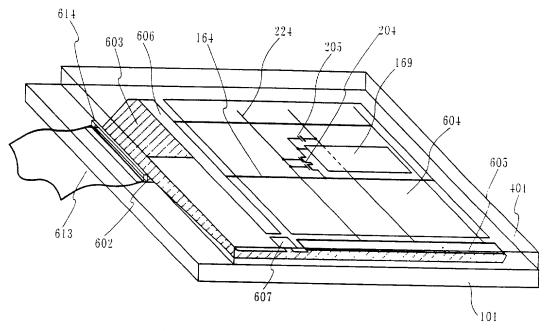


Fig.26

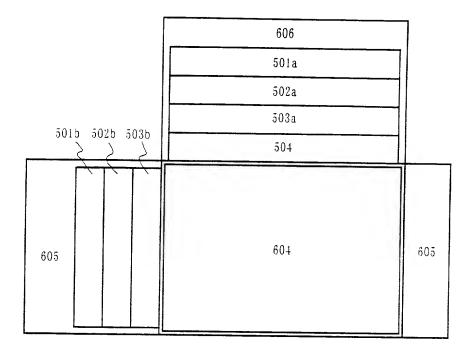
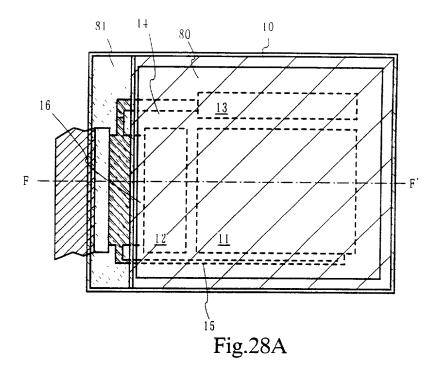
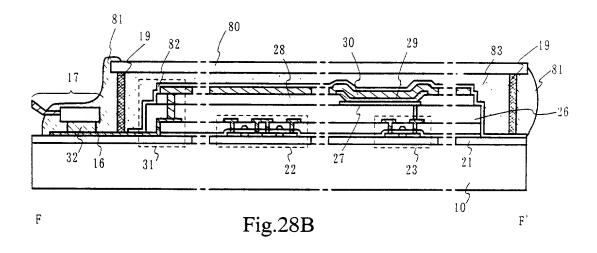
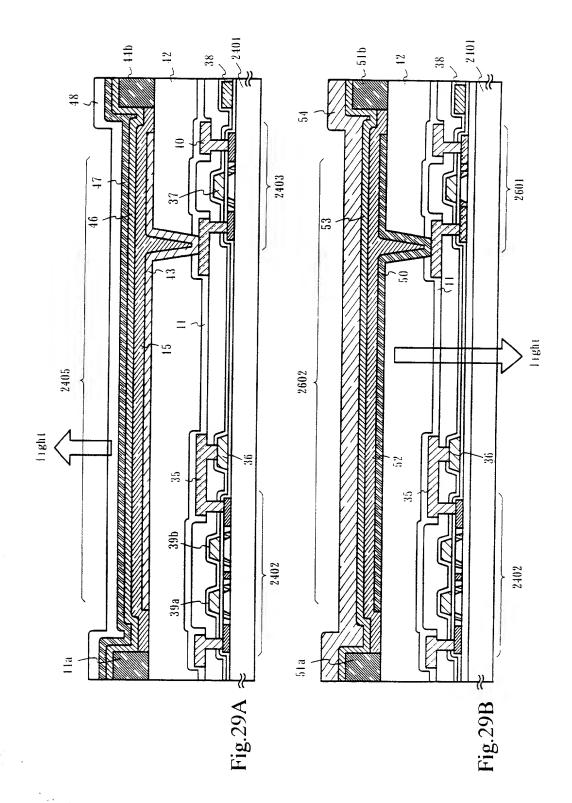
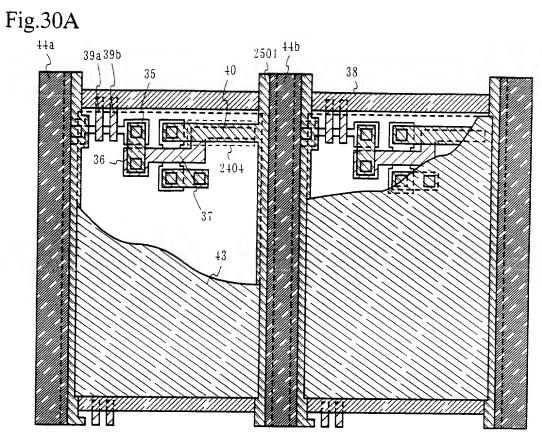


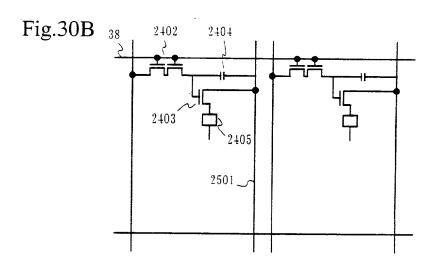
Fig.27











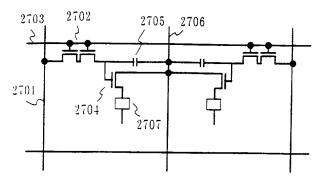


Fig.31A

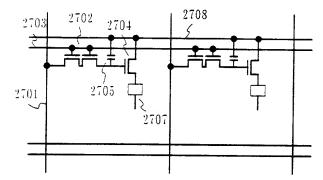


Fig.31B

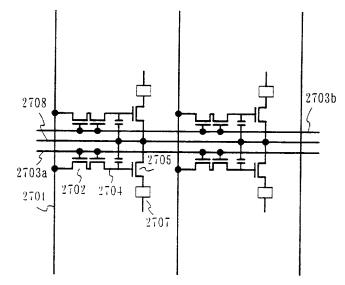
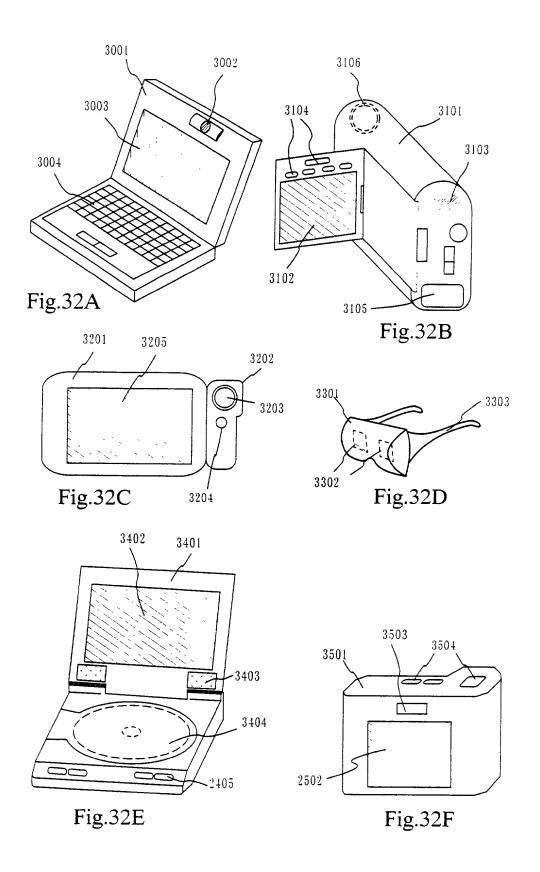


Fig.31C



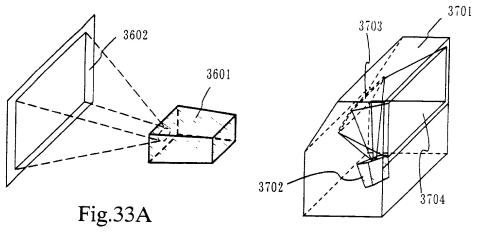
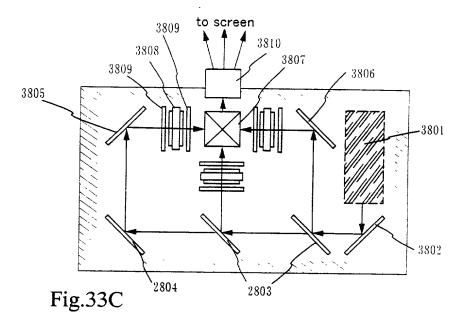


Fig.33B



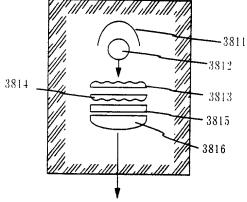
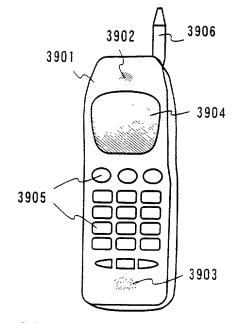
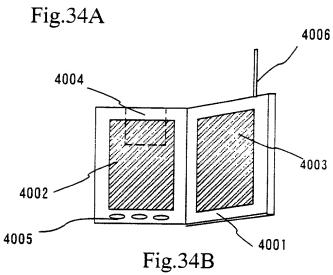


Fig.33D





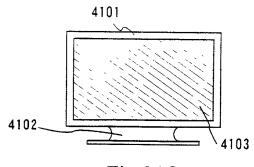


Fig.34C

Fig.35A

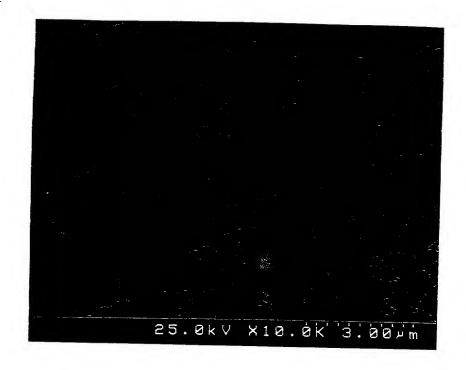


Fig.35B

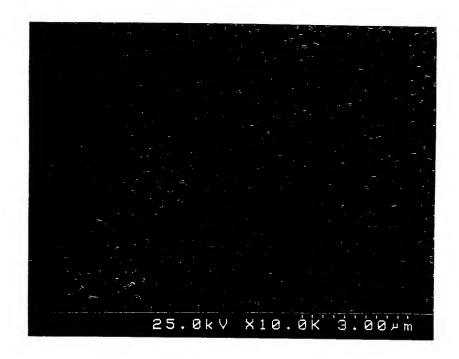


Fig.36A

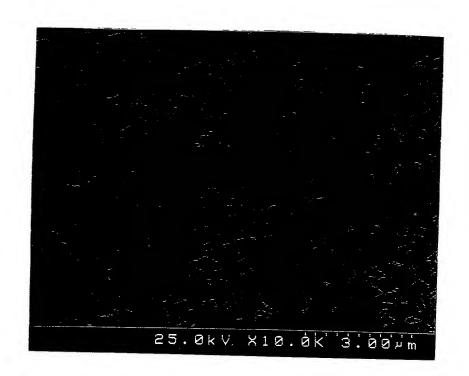


Fig.36B

